NOVEL HIGH PERFORMANCE SPDT POWER SWITCHES USING MULTI-GATE FET's

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ABSTRACT

The development of a 16 watt SPDT MESFET based switch is presented. The switch is unique in its use of a multi-gate FET device which can be fabricated on a standard production switch process. The power handling is 9 times that of a single FET while occupying only 30% more die area. The device's bandwidth is comparable to a single FET while insertion loss is minimized using a novel N-plus (N+) intergate layer. A switch using the multi-gate device has achieved 0.4dB insertion loss and 40dB of isolation at L-Band.

INTRODUCTION

A fundamental problem in device design for high power switches is to maintain acceptable insertion loss and high breakdown voltage. Power handling in an off-state GaAs MESFET is limited by voltage breakdown from the source/drain terminal to the gate terminal. Breakdown voltage can be increased by reducing doping concentration and/or increasing the source to drain spacing. Both these approaches significantly increase Ron and degrade the insertion loss. SIGFETS [1] have been used to improve breakdown voltage allowing a 6W SPDT switch to be realized. The SIGFET requires a large negative control voltage of the order of -17V for optimum power. A series combination of MESFET's has been used [2] to improve RF voltage breakdown using a chain of single gate MESFETs as capacitive voltage dividers. Up to 40 watts have been achieved using all-shunt designs and quarter-wave transformation. This approach, however precludes a single chip solution at L-Band. The series combination increases insertion loss and reduces bandwidth due to excessive shunt capacitance. More importantly this shunt capacitance does not allow an even voltage split across each device thus degrading power handling. The multi-gate structure presented here significantly reduces parasitic shunt capacitance and exhibits improved insertion loss over the series FET combination. The power handling is at least equivalent and potentially better than the series FET combination. By eliminating ohmic contact pads between the gates, the device allows for a high power, broadband RF switch to be realized with a significant reduction in die size. The approach has resulted in a 16 watt SPDT terminated switch exhibiting useful bandwidth beyond 2GHz. The switch was realized with a 50% reduction in die area over the equivalent series FET design making it useful in low-cost, high-volume commercial applications.

A multi-gate approach has been used to improve power handling in voltage variable attenuators. [3] This depends on scaling to achieve similar small-signal performance. The scaling used in [3] however omits any discussion of shunt capacitance to ground from drain and source contacts. This is a major limitation in SPDT switches and is addressed here. Dual-gate devices have also been used [4] to improve RF voltage handling. However, these devices were not optimized to improve on-resistance. Thus current handling limitations were improved by direct scaling of FET periphery. This scaling also increases shunt capacitance and reduces operating bandwidth. The structure presented here uses a unique N+ contact layer to decrease insertion loss between gates.

DEVICE FABRICATION

The devices are made using a manufacturing process based on ion implantation. The process is designed to create an epitaxial-type N+/N carrier profile while taking advantage of the high throughput and uniformity (both across the wafer and from wafer to wafer) offered by ion implantation. The three inch SI GaAs substrates are implanted with a blanket ion-beam exposure, according to a schedule that consists of a high-energy implant and a high-dose low-energy implant. After the ohmic contacts are formed, the devices are isolated using boron implantation. The 1μm long gates are self-aligned to the N+ layer and are made with optical photolithography. The gate self-alignment feature to the N+ layer makes the close spacing of the gates and relatively low device on-resistance feasible. This would be very difficult to achieve with a fabrication process based on selective ion implantation and optical photolithography. A cross section of the device is shown in Figure 1. The spacing between source and drain is

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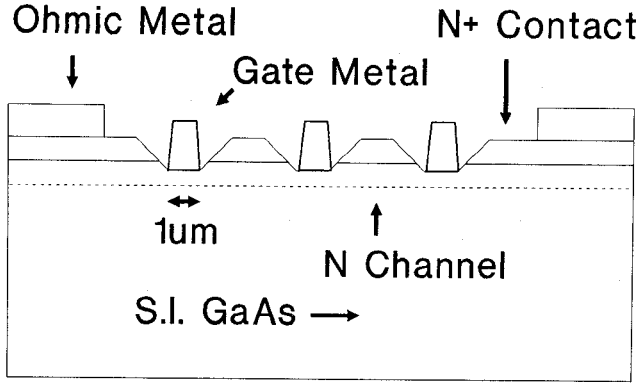


Figure 1 Cross-section of multi-gate FET.

9μm and the distance between the gates is 2μm. The devices are passivated with a 1500 Å of PECVD SiN. The device is then completed with the formation of the various interconnects. A completed device is shown in Figure 2.

ELECTRICAL CONSIDERATIONS

The multi-gate structure just described has improved performance potential over a simple series connection in insertion loss, bandwidth and power handling. Consider the simplified switch FET models of figure 3 representing a series connection of three FETs and the multi-gate FET. Insertion loss is improved since the multi-gate device has less series resistance per mm of width. Total resistances for the series connection and the multiple-gate device are;

$$R_{series} = 3\,R_{on} + 6\,R_{n^+} + 6\,R_{ohmic} = 9\ \Omega mm$$

$$R_{multi} = 3\,R_{on} + 4\,R_{n^+} + 2\,R_{ohmic} = 7.8\Omega mm$$

This represents a 14% reduction in R_{on}. It is instructive also to consider the effect of the short N+ layer between the gates. This layer has a significant impact on the on-resistance which would increase to 9.4Ωmm without it.

The improvement in operating bandwidth is evident by considering the series - shunt SPDT topology of figure 4. The effect of additional shunt capacitance in the series connected device is to increase total shunt capacitance from

$$3C_{S1} + C_{S2} + \frac{C_{off1}}{3} + \frac{C_{off2}}{3}$$

for the multi gate FET to approximately

$$5C_{S1} + \frac{C_{P1}\,C_{S1}}{C_{P1}\,C_{S1}} + \frac{C_{P2}\,C_{S2}}{C_{P2} + C_{S2}}$$

For a 3mm series FET and a 1mm shunt FET, this is equivalent to a 30% increase in shunt capacitance.

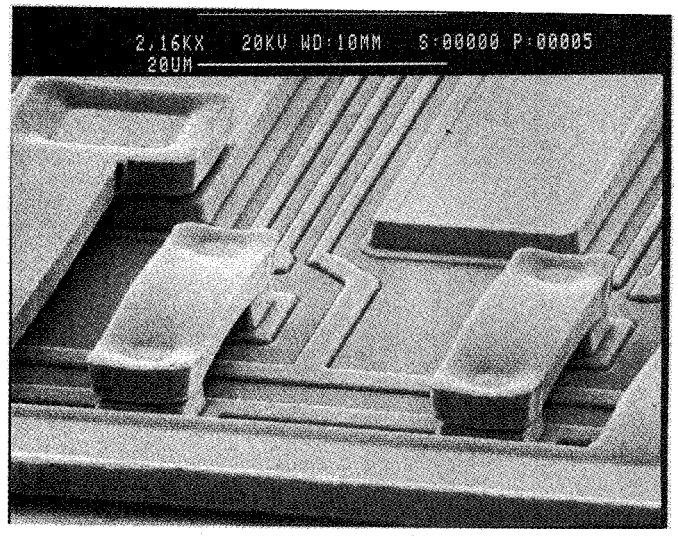
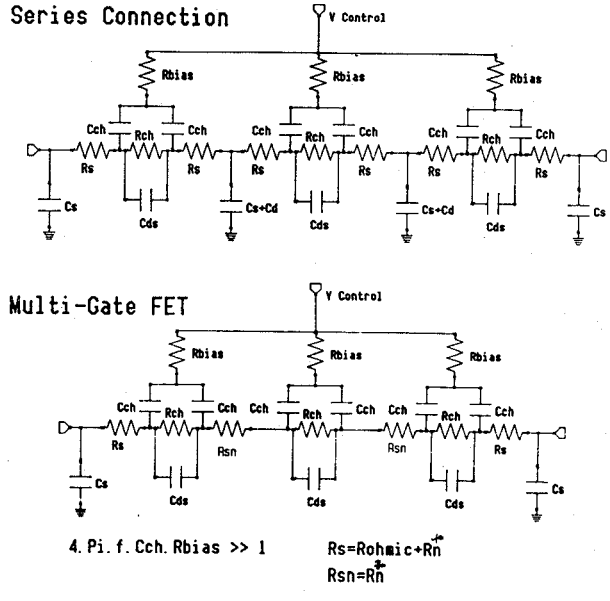


Figure 2. SEM photo of multi-gate device showing airbridges, ohmic-contacts, and multiple gates



R_{ohmic} = 0.1 ohm.mm	C_{on} = 0.8pF/mm
R_{n^+} = 0.4 ohm.mm	C_{off} = 0.2pF/mm
C_S = 30 fF/mm	R_{on} = 2.0 Ohm.mm
C_D = 30 fF/mm	R_{off} = 5.0k ohm.mm

Figure 3. Equivalent circuits for series FETs and multi-gate structure

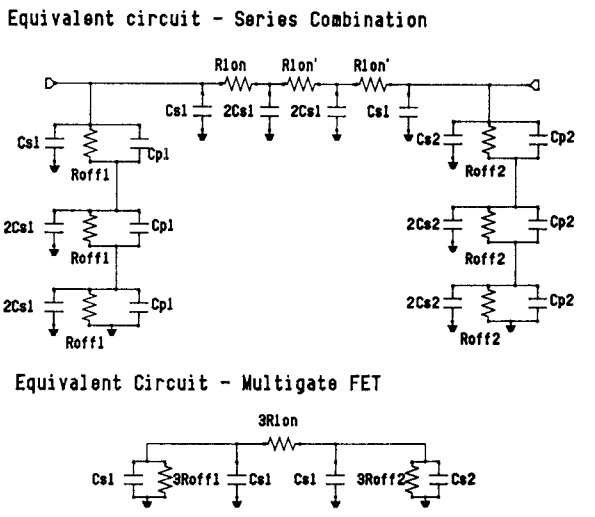


Figure 4. Small signal models for Series connection and multi-gate SPDT switch

DYNAMIC BEHAVIOR

The power handling of the multi-gate design is determined by the breakdown of the drain/source to gate terminals, by the electrical asymmetry of the shunt FET and the gate to source leakage current. It is assumed that the FET periphery is wide enough to handle the on-state current. A first order voltage swing is determined in accordance with reference [2] as

$$V_{max} = n \cdot (V_B - V_P)$$

and

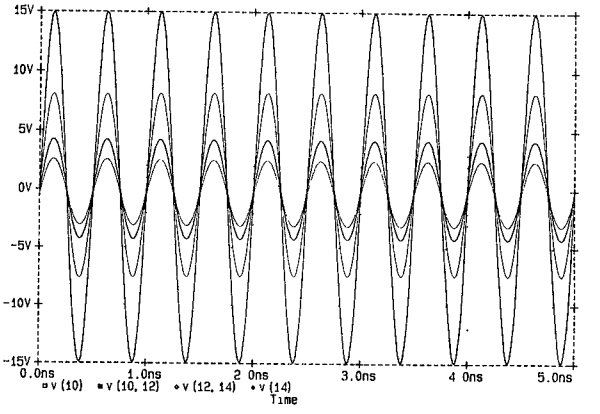
$$V_{bias} = (V_B + V_P) / 2$$

where

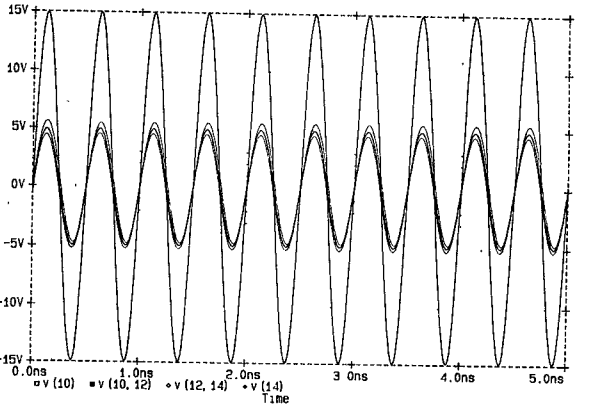
V_P is the pinch-off voltage
V_B is the breakdown voltage
n is the number of gates

Provided the gate bias resistor value is high enough the RF voltage will split equally across the depletion region under each gate in the multi-gate FET. The total power handling in a 50 ohm system if V_P = -2V and V_B = -16V is 17.6 watts. We have measured 16 watts at 1dB compression for a triple gate device. Since there is little or no fringing capacitance to ground from the N+ layers between the gates, electrical symmetry is guaranteed for the triple gate structure. A series connection of FETs however has different impedance to ground at each successive drain node as evidenced by inspection of Figure 4. This causes unequal splitting of the RF voltage with more going to the FET connected to the RF line. This FET is consequently the first to breakdown. Figure 5 shows the non-linear voltages developed in both structures clearly demonstrating the superiority of the multi-gate FET. As can be seen the peak RF voltage is three times higher for the depletion region closest to the RF source. For the multigate structure, the RF voltage is within ±10% for all three depletion regions.

Leakage current in both structures can cause effective re-biasing at the gate terminal during RF voltage swing. To maintain high power handling both the gate resistor value and the control voltage should be large. A non-linear FET model should include FET capacitance as a function of bias, channel to gate breakdown voltage and leakage current. A modified statz model can be used to simulate the dynamic behavior of the multi-gate device by including an additional pair of anti-parallel diodes across the gate/drain and gate/source terminals.



a) Series Connected FET



b) Multi-gate FET

Figure 5. a) Unequal voltage splitting in the series connected device and
b) Its elimination in the multi-gate structure

APPLICATIONS

A SPDT series-shunt switch has been implemented with multi-gate devices. The switch exhibits better than 0.8dB insertion loss to 3GHz at all control voltage levels. Figure 6 shows the small-signal characteristics of the device. The device is capable of impressive low distortion and high power operation. Figure 7 shows a measured 1dB compression point of 16 watts for a control voltage of -12V. The harmonic content at this drive level is shown in Figure 8. All harmonics are 30dB below the fundamental. Since the pinch-off voltage is -2.5V, enhanced power performance is achieved even with a -5V control. The 1dB compression at -5V is 3 watts with at least 25dB suppression of all harmonics.

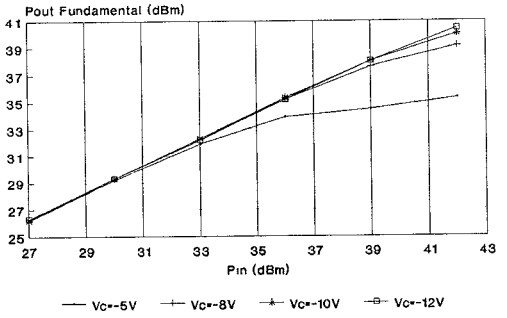


Figure 7. Fundamental output power versus input power.

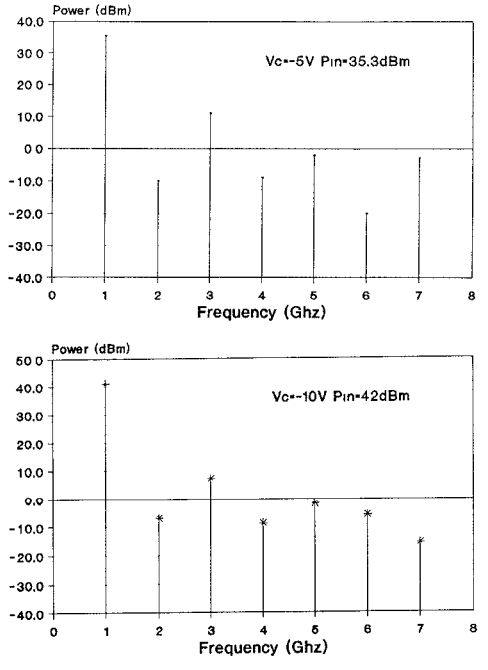


Figure 8. Harmonic content for V_C = -5V and -8V

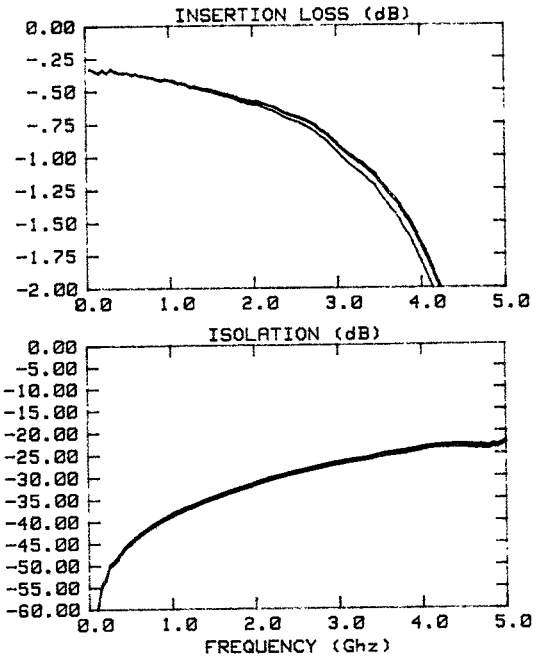


Figure 6. Measured insertion loss and isolation of multi-gate SPDT switch (V_C = -5V, -8V, -10V)

CONCLUSION

Multiple-gate fets have been used to significantly increase the power handling and distortion characteristics of SPDT switches. A 16 watt switch has been presented which can be fabricated with a standard production switch process on a 1.3 x 1.3mm^2 die.

ACKNOWLEDGEMENTS

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